

WHITE RABBIT TIMING & TRIGGERING SYSTEM

Reliable precise time with synchronized
triggers and gate signals for High Energy Facilities



Accurate White Rabbit based timing and synchronization for the proper functioning, optimization, and safety of particle accelerators. The High Energy Physics White Rabbit Timing System is a standalone device with 7 configurable inputs/outputs SMA ports to provide the generation of synchronized triggers and gate signals at a delay resolution below 10ps and output peak to peak jitter below 100ps. The system allows total flexibility when configuring the triggers in terms of direction, number of pulses, pulse rate, pulse width, pulse period and delay.

The Timing System integrates our HATI IP core, allowing for sub-nanosecond synchronization between a WR based master device and several slaves.

- Sub-nanosecond time accuracy
- 7 configurable input/output ports
- Very high scalability and large distance links support
- FPGA based hardware
- Nanosecond timestamping
- Nanosecond control
- High Accuracy Timing IP Core (HATI)
- Trigger Generation
- Event Counter
- EPICS Controls
- Central Management Console

Safran Electronics & Defense is with you every step of the way, building in the intelligence that gives you a critical advantage in observation, decision-making and guidance.

High Accuracy

The HATI (High Accuracy Timing IP) is a FPGA core intended to enable sub-nanosecond synchronization accuracy once it is integrated onto a third-party hardware that it is connected to a Safran's WR-Z device by using optical fiber links. The IP core is able to achieve this performance thanks to the use of White Rabbit protocol (based on IEEE-1588, Sync-E and precise clock compensation).

FPGA Based

The WR devices are powered by FPGAs, therefore their hardware can be easily reprogrammed and kept up to date.

WR Based

Compatible with White-Rabbit and IEEE-1588 protocols. Seamless integration with our control and monitoring devices like LLRF and BPM.

Configurable triggers/gate signals

The timing system allows the generation of fully configurable triggers signals. Parameters such as the repetition rate, pulse period, pulse width, polarity and number of pulses can be configured individually for each port using the GUI.

Event Counter

The system can operate as an event counter when configuring the ports as inputs. Minimum pulse width configurable to avoid false detections.

Nanosecond timestamping

The core HATI provides a common sense of time to all the nodes connected to the WR network allowing the timing system to perform event timestamping with precision in the order of nanoseconds.

High scalability

The WR technology allows the possibility of adding new nodes to the network without any extra work required.

The nodes keep synchronization over distances in the order of tens of kilometers.

No calibration needed

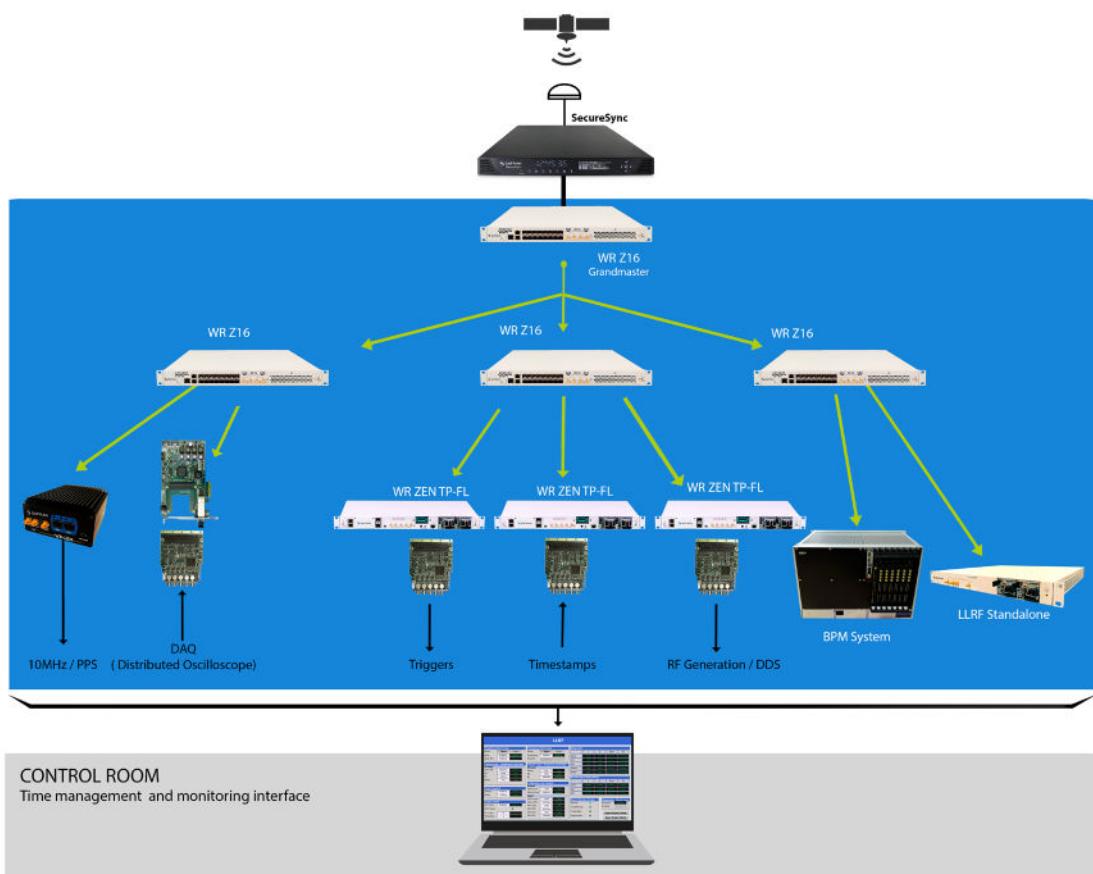
The WR technology performs automatic link calibration.

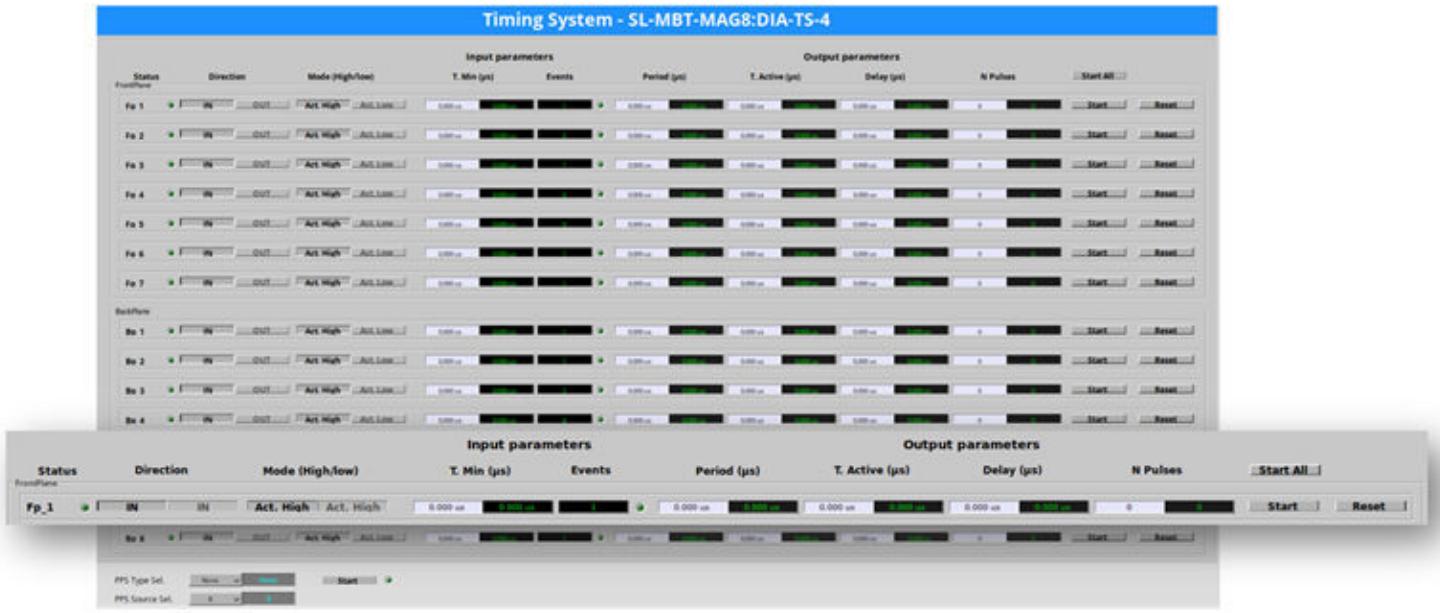
EPICS based

EPICS control system support and intuitive graphic user interface (GUI) to configure and monitor the operation of the system.

Timing Distribution Options

The timing system can operate using various timing distribution methods. White Rabbit based Z16 is recommended for White Rabbit networks. An RF Frequency reference can also be used.





Technical Specifications

System on Chip	
SoC	Xilinx Zynq Ultrascale+ series
CPU	Quad ARM® Cortex™-A53 1.5GHz
Memory	8GB DDR4 16 GB SD card

Physical Specification	
Dimension	44.45 mm x 482.6 mm x 372.85 mm
Color	RAL9002

Time Sync Characteristics	
• 7 x configurable input/output 3.3V LVCMOS (SMA connector)	
• PLL for low phase noise distribution clocks	
• 8GB DDR4 for processor and data storage (postmortem analysis)	
• ETH & SFP port (White Rabbit compatible)	
• uTCA MMC controller	
• Fail-safe for overheating mode	
• uSD socket, uUSB port.	

Environmental Conditions	
Temperature	-10°C ~ +50°C
Humidity	0% ~ 90% RH

Triggering Characteristics	
Repetition rate	0.1Hz to 10MHz
Delay	5ns to 10s (5ns step)
Pulse width resolution	5ns
Polarity	Selectable high/low
Pulse burst	1 to infinite pulses
Fine Delay	Below 10 ps

Management	
OS	Linux (Kernel v4.14 & buildroot)
Control	EPICS/TANGO
Monitoring	CSS/GUI & Taurus

Timestamping Characteristics	
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Performance	
Resolution	5 ns
PPS stability*	< 300ps (peak to peak) < 60ps (std. dev)

*Long term measures between master PPS from a WR-Z16 and slave PPS.

Event Counter Characteristics	
Maximum pulses count	2^{32}
Pulse minimum width configurable for detection	5ns to 10s (5ns step)

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